Synthesis of FET based full-Heusler alloy thin films formed by rapid thermal annealing and transport properties

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Abstract. In this work we show a preparation technique of Co_2FeSi full-Heusler alloy thin films on silicon-on-insulator (SOI) substrates, employing rapid thermal annealing (RTA). The films of the Co_2FeSi alloy were formed by a silicidation reaction, caused by RTA, between the ultrathin SOI (001) layer and the Fe/Co layers deposited on it. It is assumed that this technology is compatible with the process of formation of a half-metal source-drain in an advanced CMOS and SOI technology and will be applicable for the manufacture of a source-drain of a field-effect transistor. Schottky barrier field-effect transistors (FET) with a back-gate, based on silicon nanowires with source and drain of a Co_2FeSi film, synthesized on an SOI substrate, were manufactured. The transport properties of the device are investigated.

1. Introduction

Promising is the research and development of spintronics devices that will allow the use of both electronic charge and spin degrees of freedom for the transmission, storage and processing of information. Good candidates for application as ferromagnetic (FM) injector is iron silicide Fe_3Si [1] or half-metallic full-Heusler alloys containing Si (Co_2MnSi [2], Co_2FeSi [3], etc.). Last is one of attractive candidates for spin MOSFETs with the HMF source/drain, since these materials are considered to be a kind of silicides and thus they have a possibility to be formed by the RTA-induced silicidation process. Use of Schottky barrier field-effect transistors [4] geometry, avoids the need for doping by replacing the source / drain transitions with metal / semiconductor transitions, leaving the nanowire undoped [5]. In contrast to bulk and thin film devices by using silicide sharp transitions metal / nanowire [6] can be achieved. Consequently, local changes in the contact area as well as in geometry are avoided. The ability to form devices using silicon-on-insulator (SOI) substrates allows this technology to be fully integrated into integrated electronic systems. Allowing taking full advantage of the selected geometry of the transistor and the silicidation technology.

2. Experimental

Nanowire devices are formed on boron doped silicon on insulator (SOI) substrates (with resistivity of 18 Ω·cm) using e-beam lithography and wet and dry etching with help of Raith VOYAGER e-beam writer and NORDSON MARCH RIE-1701 anisotropic reactive ion etch plasma system. Nanowire channels of various widths were formed from the top layer of the SOI substrate, using electron lithography in combination with anisotropic reactive ion etching. For the formation of source and

drain, Co and Fe films were deposited sequentially and rapid thermal annealing was carried out to form the silicide Co_2FeSi. The pads of the Co_2FeSi alloy were formed by a silicidation reaction, caused by RTA, between the ultrathin SOI (001) layer and the Fe/Co layers deposited on it. As a result, the device is a silicon nanowires with half-metal drain and source (Figure 1a- inset). To create the back gate of the field-effect transistor, an ohmic contact of indium was formed on the back side of the SOI substrate.

3. Results and discussion

The devices obtained measured the transport properties in EMPX-HF probe station (Lake Shore cryotronics). For Co_2FeSi / SOI back-gate nanowire transistor transport properties were studied. Transfer characteristics demonstrates behavior like pseudo MOSFET or nanowire FET with Schottky source/drain contacts. The preliminary transport measurements of the device obtained, as can be seen from Figure 1, demonstrate the typical behavior of a field effect transistor.

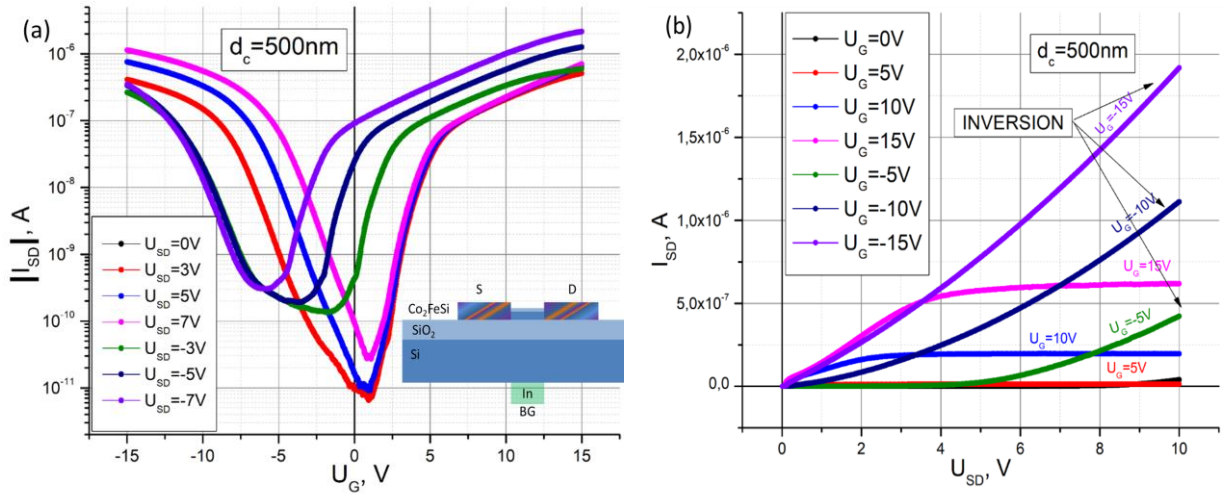

Figure 1(a, b). (a) The transfer characteristics Co_2FeSi/SOI back-gate nanowire transistor with a channel width of 500 nm plotted on a semilog scale at different voltages on source-draine; **(b)** Output characteristics device in inversion and accumulation mode.

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