Pseudorandom Sequence Generator Using CORDIC Processor

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***Abstract*— The article describes the formation of a pseudorandom sequence using the CORDIC processor. The principle of pipeline implementation of computations is disclosed and structural schemes for the formation of a pseudorandom sequence in the LabVIEW programming environment are given.**

Keywords*— *Pseudorandom sequence, CORDIC processor, computing pipeline, Code Division Multiple Access

I. INTRODUCTION

Currently, the wireless network is under increasing pressure. These are voice communication, wireless data transmission, wireless Internet. At the same time, an increase in the capacity of wireless networks is possible mainly only due to multiple access [1]. Multiple access is a radio transmission scheme that allows several earth stations to operate simultaneously, which makes it possible to integrate these stations into a Star or Mesh network.

One of the popular standards of multiple access is Code Division Multiple Access (CDMA) [2, 3]. This standard is applied in many areas of wireless communications, including space [4]. ViaSat's ArcLight CDMA system is used to provide broadband mobile satellite services on board a variety of vehicles, including airplanes, ships, and high-speed trains. In its structure, standard transmitting and receiving equipment is successfully combined with the revolutionary proprietary technologies ViaSat, which include increased efficiency of the direct channel with ACSM (Adaptive Coding, Spreading and Modulation) technology, as well as CRMA (Code Reuse Multiple Access) and A-PCMA technologies (Asymmetric Paired Carrier Multiple Access).

In CDMA, there are no restrictions on frequency and time. The principle of CDMA is that each source of information is assigned an individual code with which it encodes the transmitted message. The receiver of the information also knows this code and its task is to extract the coded message of the desired sender from the entire stream of other messages. That is, each transmitter modulates a signal using a separate numeric code assigned to each user at the moment, and the receiver calculates the necessary part of the signal using a similar code [5]. The principle of code data separation is shown in Figure 1.

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In CDMA, each transmitted bit of information is encoded with several bits of the spreading sequence using a logical XOR operation. Such an operation is called an extension. As a spreading sequence is most commonly used pseudo-random sequence.

II. DIGITAL PSEUDORANDOM SEQUENCE GENERATION

One of the main problems that must be addressed when developing high-speed CDMA communication systems is the problem of forming a pseudo-random sequence.

The hardware basis for the formation of the digital code of the modulating sequence is the FPGA. To date, to generate signals with its code pseudo-random sequence, vector signal generators are mainly used, in which the modulating sequence is formed by reading from memory or in real time. The process of signal generation consists in creating quadrature components, the law of time variation of which corresponds to the polynom code sequence and modulating this sequence of digital information of the transmitted message.

There are several basic FPGA architectures, each of which has an advantage either in speed of work or in ease of implementation. However, the development of computational architectures operating at 100–200 MHz is necessary to pipelining the computations. Despite the fact that the pipeline architecture has a large overhead of aligning the delays of the computing blocks, its use is justified in processing and converting complex signals.

Using a CORDIC processor, which is identical in hardware resources to a pipeline processor and operates in rotation mode, allows you to immediately get the quadrature components of the pseudo-random sequence of the $I(t)$ and $Q(t)$ signal [6, 7].

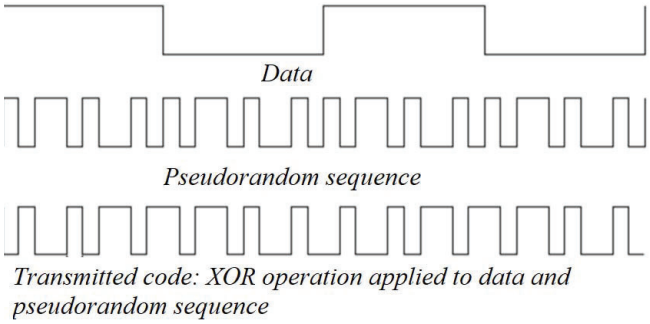

Fig. 1. The principle of code data separation

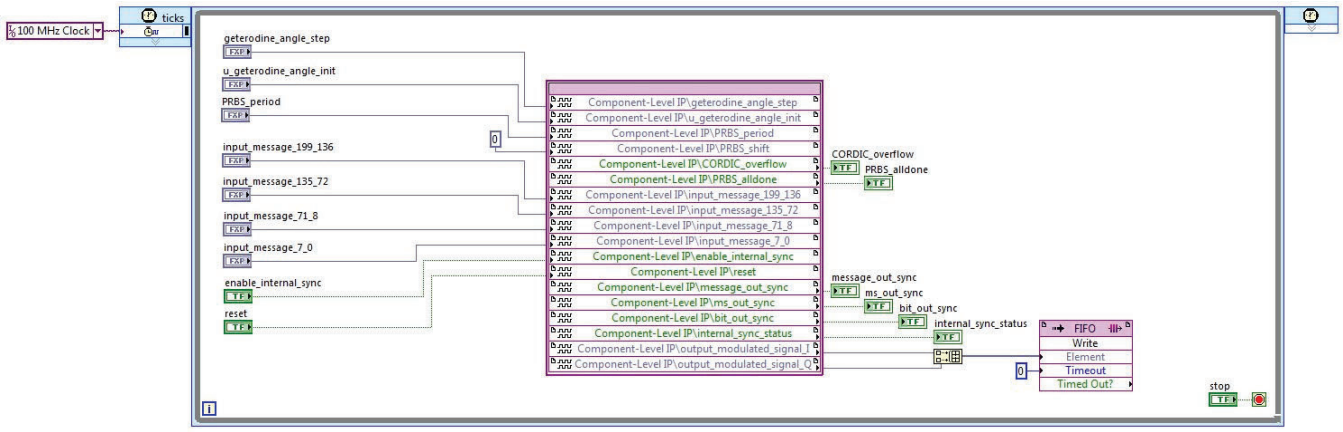

Fig. 2. Pipelined implementation of a CORDIC processor for calculating $I(t)$ and $Q(t)$

CORDIC processor operates according to the expression:

$$\begin{aligned} x^{(i+1)} &= x^{(i)} - d_i y^{(i)} 2^{-i}, \\ y^{(i+1)} &= y^{(i)} + d_i x^{(i)} 2^{-i}, \\ z^{(i+1)} &= z^{(i)} - d_i \tan^{-1} 2^{-i} \end{aligned} \quad (1)$$

where $x = \cos(z)$, $y = \sin(z)$, z – target angle, $d_i = \text{sign}(z^{(i)})$, d∈ {–1, 1}.

To speed up the calculation of the angle of rotation of the signal vector, intermediate values of $\tan^{-1}2^{-i}$ are pre-calculated and stored in registers. At each iteration, the sign of the intermediate angle value is checked, then the angle increment is selected at the next iteration of the conveyor.

The pipeline implementation is capable of operating at a frequency of more than 100 MHz and allows you to calculate the values of $I(t)$ and $Q(t)$ per cycle. Figure 2 shows the block diagram of the pipeline implementation of the CORDIC processor.

The digital generation of CDMA signals allows the use of various standards and formats of message frames. This is achieved by separating the pseudorandom sequence forming units and the digital message.

Figure 3 shows a block diagram of the formation of CDMA signals. All blocks in the diagram are synchronized with each other using a block of generating synchronization signals.

LabVIEW's flexible software architecture allows you to program the necessary ensemble of a pseudorandom sequence and then automatically compile the LabVIEW vi code into VHDL to implement the FPGA logic (Figure 4).

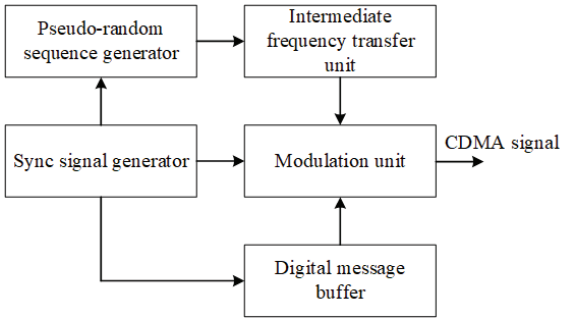

Fig. 3. The block diagram of CDMA signal generator

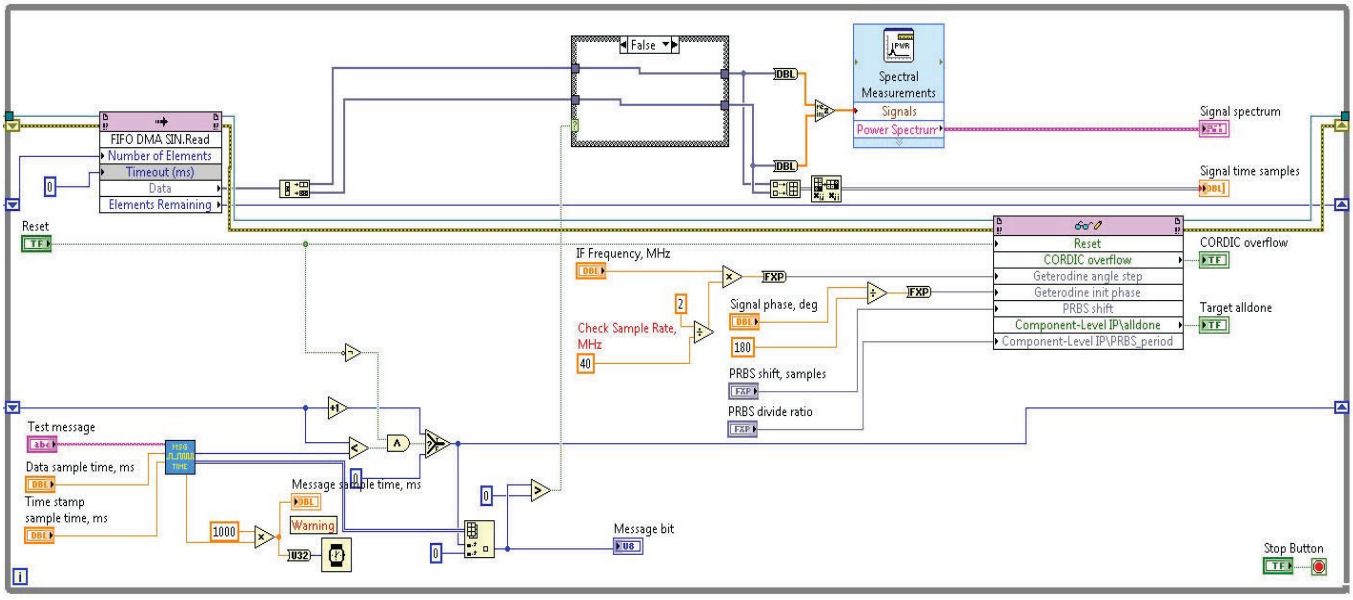

Fig. 4. LabVIEW VI CDMA signal shaper block diagram

To form a pseudorandom sequence, a shift register and a block of logical summation Mod 2 are used. The formation is carried out in a generation block (Figure 5).

The inputs of the logic adder Mod 2 served bits 5 and 9 of the shift register. The result of modulo 2 is fed to the input of the shift register in bit 1. The pseudo-random sequence is removed from 8 bits of the shift register.

The generated pseudo-random sequence is transferred to the intermediate frequency in the transfer unit to the intermediate frequency using a lettered frequency generator based on the CORDIC harmonic signal generator with a continuous phase [8] and a quadrature modulation scheme by code (Figure 6).

The CORDIC harmonic signal generator is synchronized with the FPGA clock pulses with a frequency of 100 MHz and outputs a quadrature signal with a 50 MHz spectrum width. The frequency value is set in 6103.5 Hz steps. A quadrature signal at a given intermediate frequency is fed to the inverter for parallel formation of a negative signal value and input to the selector, together with a positive signal value.

The selector switches the current value of the harmonic signal in accordance with the value of the bits of the pseudorandom sequence. It is also synchronized with pseudorandom sequence clock pulses.

The generated pseudo-random sequence signal at an intermediate frequency is modulated by a digital message. Its samples are pre-buffered and synchronized with a common clock signal on the FPGA in the modulation unit (Figure 7).

Buffering is performed by the synchronization signal of the digital message, which is generated on the FPGA in the synchronization signal generation unit. Buffering stores the string data of a digital message in a buffer for progressive, synchronized with a pseudo-random sequence, of data transmission in a modulation unit. Thus, at the output, a sequence is formed corresponding to the structure of the CDMA signal.

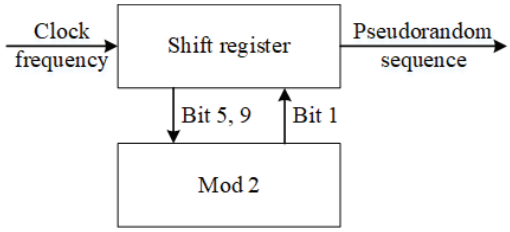

Fig. 5. Pseudorandom sequence generation block

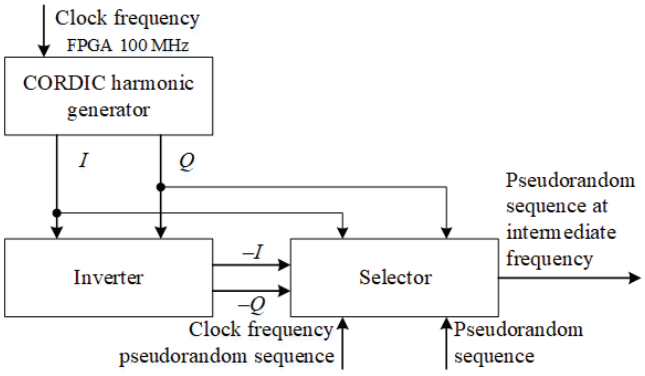

Fig. 6. Intermediate frequency transfer unit

Figure 8 shows the front panel for controlling and monitoring the parameters of a CDMA signal. The test digital message is written to the FPGA buffer. On the dashboard, it is possible to set the value of the intermediate frequency of a pseudo-random sequence, the initial phase of the harmonic signal generator, the clocking parameter of the pseudo-random sequence from the clock frequency of the FPGA, on / off use of the sync signal generation unit, resetting the hardware blocks.

III. Hardware Implementation of the CDMA Signal Generator

To reduce the time and cost of developing a hardware implementation, it is advisable to use modular equipment. For example, such PXI modules manufactured by National Instruments, such as: vector generators, analyzers, programmable FPGAs, DACs and ADCs. These modules fully meet the requirements for creating CDMA signals of various structures and their generation into the propagation medium.

The prototype of the shaper CDMA signals at an intermediate frequency is implemented on the NI FlexRIO PXIe-7976R module based on the Xilinx K710T FPGA (Figure 9). This FPGA in digital signal processing tasks provides maximum flexibility. The digital code of the generated signal is converted into an analog signal by a DAC.

The in-phase and quadrature components of the analog signal from the DAC output are filtered by a low-pass filter and fed to the output of the arbitrary waveform generator. The NI PXIe-5673 vector signal generator uses direct signal transfer from the baseband to the radio frequency range. The in-phase and quadrature components of the CDMA signal and the continuous RF signal at the carrier frequency from the high-frequency generator NI PXI-5652 come to the input of the NI PXIe-5611 vector modulator [9].

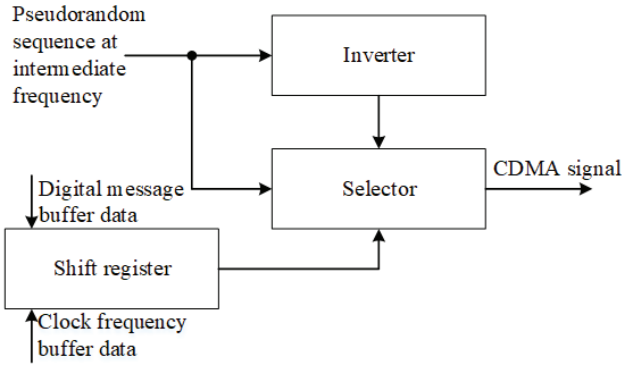

Fig. 7. Modulation unit

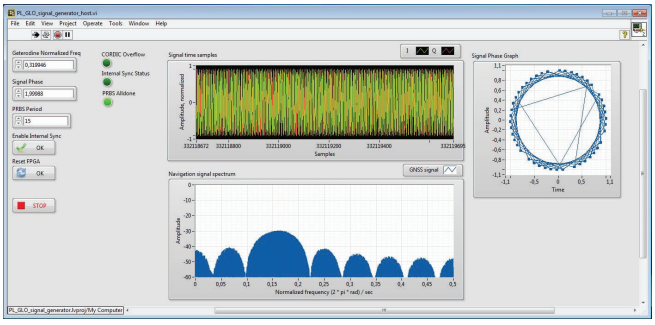

Fig. 8. LabVIEW front panel control and monitoring of CDMA signal parameters

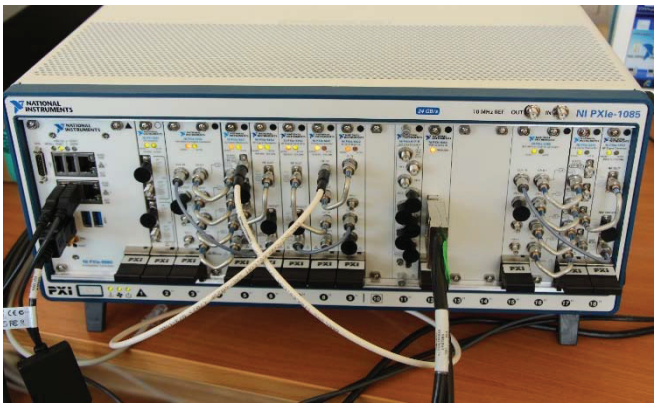

Fig. 9. Appearance of equipment for generating CDMA signals

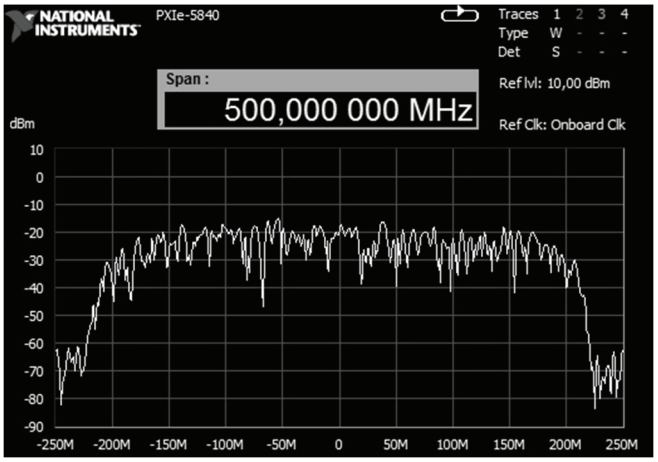

Fig. 10. Radio frequency spectrum of the generated CDMA signals

The parameters of this vector generator provide the required characteristics of the spectrum of the emitted CDMA signals (Figure 10).

IV. Conclusion

Thus, the use of a CORDIC processor allows you to immediately obtain the quadrature components of a pseudorandom signal sequence at frequencies above 100 MHz. The CORDIC processor for hardware resources is identical to the pipeline processor and operates in the rotation mode. The given software and hardware implementation allows generating pseudorandom sequences based on various polynomials and generating CDMA signals of a given structure. The flexible control of the modular elements of the software-hardware complex ensures the formation of a given frequency-code structure and power of the emitted CDMA signals.

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